REMARKS/ARGUMENT

This is a reissue of U.S. Patent 6,337,591.

In the Amendment filed December 31, 2003, the erroneous final paragraph of claim 1 was deleted, for the reasons explained in the Reissue Declaration, and remains deleted herein.

In the present Amendment, claim 1, line 4, is being amended by changing "temperature offset drift" to - - offset voltage temperature drift - -. This amendment does not change the scope of the claim, but merely clarifies the claim language in accordance with claim 2 and column 4, lines 25-27 in the '591 patent.

Claims 1-4 were rejected as being obvious over Parry et al. '435 in view of Okada (JP'636). The Examiner cited Okada as disclosing the claimed "circuit to minimize inherent temperature offset drift" in claim 1.

Claim 1 is being amended to include the feature of claim 2, which is being canceled. As such, claim 1 now recites that the circuit that minimizes offset voltage drift comprises a first pair of mirrored MOSFET's. As explained at col. 4, line 8, this function is performed in the disclosed embodiment by the MOSFET's 82 and 84. These in turn are the MOSFET's that provide the differential inputs VN, VP to the amplifier circuit 80. Hence, the offset voltage is equal to the difference between the respective g-s voltages of the MOSFET's. To further identify the MOSFET's in question, new claim 5 depends from claim 1 and recites, "wherein said first pair of mirrored MOSFET's receive said differential analog input signal." See also claim 7.

Claims 1 and 5 are neither disclosed nor made obvious by Parry and Okada. The Examiner argued that the MOSFET pair of claim 2, now included in claim 1, corresponded to Okada's MOSFET's Tr2 and Tr3, "such that the circuit has an offset voltage which is equal to the difference ... and remains constant over temperature variations." There is, however, nothing in Okada to indicate that the MOSFET's Tr2 and Tr3 would play any role in determining the voltage offset, since they are not disposed at the input of the amplifier circuit. Nor is there any indication that they are matched (mirrored) such that their respective gate-source voltages play the role recited in claim 1.

Allowance of claims 1 and 5, as well as dependent claims 3, 4 and 7, is therefore requested.

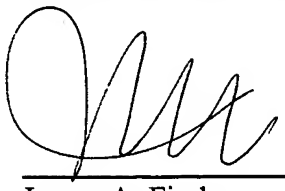
New claims 6-8 are submitted to further clarify the relationships between the disclosed MOSFET's.

Claim 6 recites a second pair of mirrored MOSFET's connected respectively in series with the pair of claim 1, for equalizing current and biasing of said first-pair. See col. 4, lines 10-12. Claim 6 is readable for example on the MOSFET's 86 and 87. There is no disclosure in Okada of a mirrored MOSFET pair having the claimed features.

Claim 8 is readable on the MOSFET's 88 and 89 as explained at col. 4, lines 14-17. No such feature is seen in Okada.

Therefore, allowance of claims 1 and 3-8 is requested.

Respectfully submitted,



James A. Finder
Registration No.: 30,173
OSTROLENK, FABER, GERB & SOFFEN, LLP
1180 Avenue of the Americas
New York, New York 10036-8403
Telephone: (212) 382-0700

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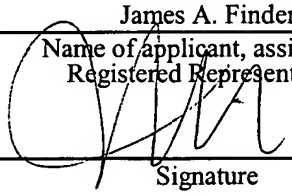

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